CLAIMS

1. A comparison circuit for an analog/digital converter comprising a network of comparators (C) each comparing an analog voltage (V) to be converted with a reference voltage (Vref), the reference voltages (Vref) being distributed over a range in which the analog voltage (V) can vary, each comparator (C) comprising a direct output (O) and an inverse output ($\overline{O}$), characterized in that each output, direct (O) or inverse ($\overline{O}$), is linked to the input of a voltage follower (A), the outputs of each voltage follower (A) being connected either to inputs of a first network (2) of resistors (R1 to R8) delivering at its outputs (O'), mean voltages that are the average of those present on direct outputs (O) of the comparators (C) receiving reference voltages (Vref) similar in their distribution over the range, or to inputs of a second network of resistors delivering at its outputs ($\overline{O}$'), mean voltages that are the averages of those present on inverse outputs ($\overline{O}$) of comparators (C) receiving reference voltages (Vref) similar in their distribution over the range.

2. The comparison circuit as claimed in Claim 1, characterized in that the outputs (O') of the first network (2) of resistors are connected, by way of voltage followers (A), to inputs of a third network (3) of resistors (R1 to R8) delivering at its outputs (O''), mean voltages that are the averages of those present on neighboring inputs of the third network (3) of resistors, and in that the outputs ($\overline{O}$') of the second network of resistors are connected, by way of voltage followers (A), to inputs of a fourth network of resistors delivering at its outputs ($\overline{O}$''), mean voltages that are the averages of those present on neighboring inputs of the fourth network of resistors.

3. The comparison circuit as claimed in one of the preceding claims, characterized in that the networks (2, 3) of resistors have the same structure.

4. The comparison circuit as claimed in Claim 3, characterized in that each network of resistors comprises a first series assembly of two identical pairs of two identical resistors in series, (R1, R2), on the one hand, (R3, R4) on the other hand, and a second series assembly of two identical pairs of two identical resistors in series (R5, R6) on the one hand, (R7, R8) on the other hand and in that the inputs of the network of resistors are constituted by the ends and the midpoint of the first series assembly, and the outputs of the network of resistors are constituted by the ends and the midpoint of the second series assembly, the midpoint of the first pair and of the second pair of resistors of the first assembly are connected respectively to the midpoint of the first pair and of the second pair of the second assembly.